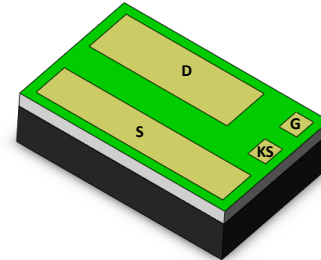
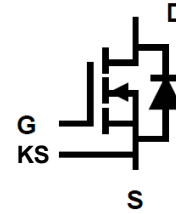


General Description

- Ultra High Switching Frequency
- Ultra Low $R_{DS(on)}$
- Fast and Controllable Fall and Rise Time
- Zero Reverse Recovery Loss
- Ultrathin and High Reliability LGA Package.
- Kelvin Source



Package: FCLGA
 Size: 1.9 mm x 2.9 mm

Applications

- Synchronous Rectification
- Class-D Audio
- Envelope Tracking Power Supplies
- High Frequency DC-DC Converter

Maximum Ratings

Symbol	Parameter	Max	Unit
V_{DS}	Drain-to-Source Voltage (Continuous)	100	V
I_D	Continuous current	16	A
	Pulsed (25 °C, $T_{PULSE} = 300 \mu s$)	110	A
V_{GS}	Gate-to-Source Forward Voltage	6	V
	Gate-to-Source Reverse Voltage	-4	V
T_J	Operating Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-40 to 150	°C

Electrical Characteristics ($T_J = 25\text{ }^\circ\text{C}$ unless otherwise stated)

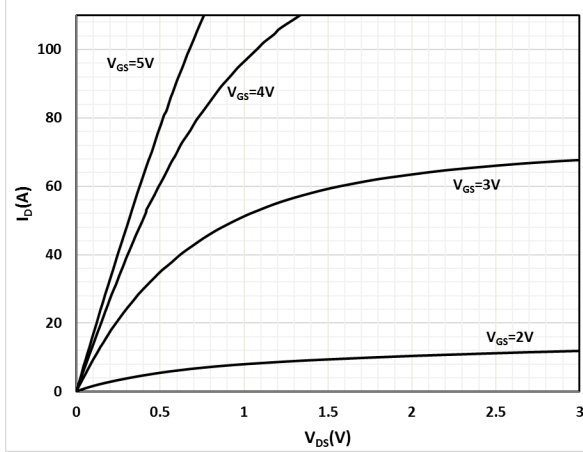
Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
Static Parameters						
BV_{DSS}	Drain-to-Source Voltage	100			V	$V_{GS} = 0\text{ V}$, $I_D = 200\text{ }\mu\text{A}$
I_{DSS}	Drain-Source Leakage		20	120	μA	$V_{GS} = 0\text{ V}$, $V_{DS} = 80\text{ V}$
I_{GSS}	Gate-to-Source Forward Leakage		1	25	μA	$V_{GS} = 5\text{ V}$
	Gate-to-Source Reverse Leakage		10	250	μA	$V_{GS} = -4\text{ V}$
$V_{GS(TH)}$	Gate Threshold Voltage	0.8	1.1	2.1	V	$V_{DS} = V_{GS}$, $I_D = 5\text{ mA}$
$R_{DS(on)}$	Drain-Source On Resistance		6	7	$\text{m}\Omega$	$V_{GS} = 5\text{ V}$, $I_D = 16\text{ A}$
V_{SD}	Source-Drain Forward Voltage		1.45		V	$I_S = 0.5\text{ A}$, $V_{GS} = 0\text{ V}$
Dynamic Parameters						
C_{ISS}	Input Capacitance		660		pF	$V_{GS} = 0\text{ V}$, $V_{DS} = 50\text{ V}$
C_{OSS}	Output Capacitance		238			$V_{GS} = 0\text{ V}$, $V_{DS} = 50\text{ V}$
C_{RSS}	Reverse Transfer Capacitance		2.6			$V_{GS} = 0\text{ V}$, $V_{DS} = 50\text{ V}$
$C_{OSS(ER)}$	Energy Related C_{OSS}		317			$V_{GS} = 0\text{ V}$, $V_{DS} = 0\text{ to }50\text{ V}$
$C_{OSS(TR)}$	Time Related C_{OSS}		443			$V_{GS} = 0\text{ V}$, $V_{DS} = 0\text{ to }50\text{ V}$
Q_G	Total Gate Charge		5.2		nC	$V_{GS} = 5\text{ V}$, $V_{DS} = 50\text{ V}$, $I_D = 16\text{ A}$
Q_{GS}	Gate-to-Source Charge		1.4			$V_{DS} = 50\text{ V}$, $I_D = 16\text{ A}$
Q_{GD}	Gate-to-Drain Charge		0.6			$V_{DS} = 50\text{ V}$, $I_D = 16\text{ A}$
$Q_{G(TH)}$	Gate Charge at Threshold		0.8			$V_{DS} = 50\text{ V}$, $I_D = 16\text{ A}$
Q_{OSS}	Output Charge		22			$V_{GS} = 0\text{ V}$, $V_{DS} = 50\text{ V}$

Thermal Parameters

Symbol	Parameter	Typ	Unit
$R_{\theta JC(top)}$	Thermal Resistance, Junction-to-Case (top)	14.7	$^\circ\text{C/W}$
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	7.7	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	48	$^\circ\text{C/W}$

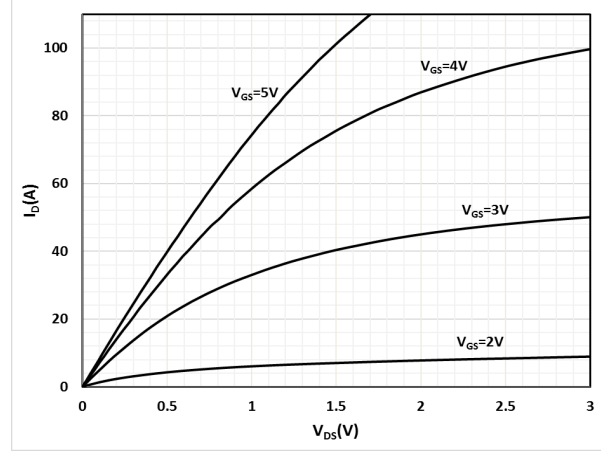
Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

Fig. 1 Typ. Output Characteristics



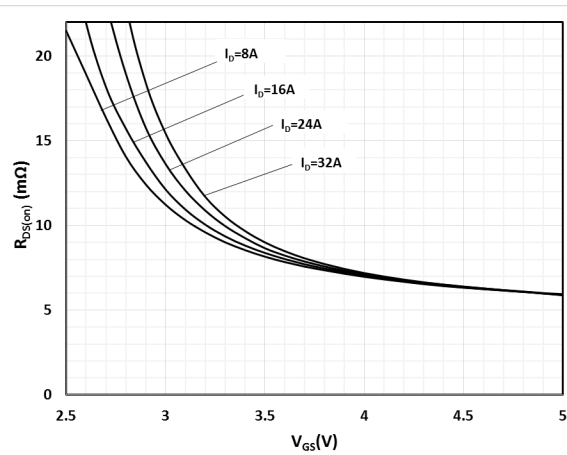
$$I_D = f(V_{DS}, V_{GS}); T_J = 25\text{ }^\circ\text{C}$$

Fig. 2 Typ. Output Characteristics



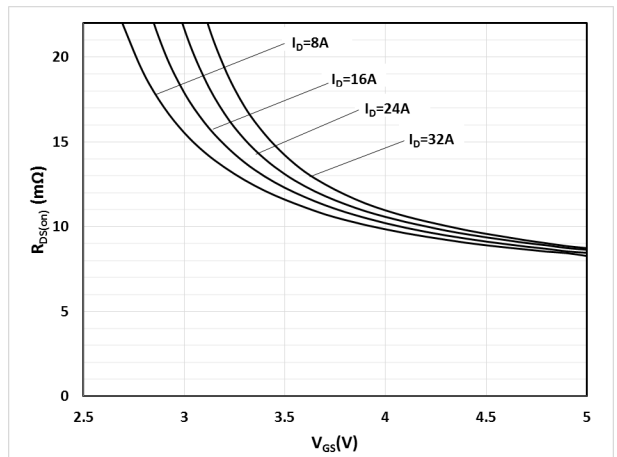
$$I_D = f(V_{DS}, V_{GS}); T_J = 125\text{ }^\circ\text{C}$$

Fig. 3 Typ. Drain-Source On-State Resistance



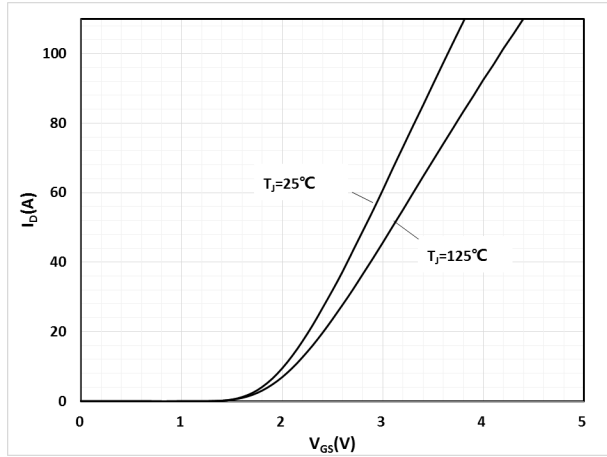
$$R_{DS(on)} = f(I_D, V_{GS}); T_J = 25\text{ }^\circ\text{C}$$

Fig. 4 Typ. Drain-Source On-State Resistance



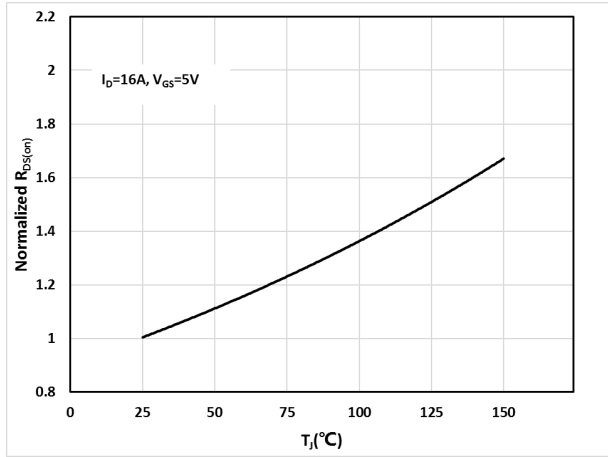
$$R_{DS(on)} = f(I_D, V_{GS}); T_J = 125\text{ }^\circ\text{C}$$

Fig. 5 Typ. Transfer Characteristics.



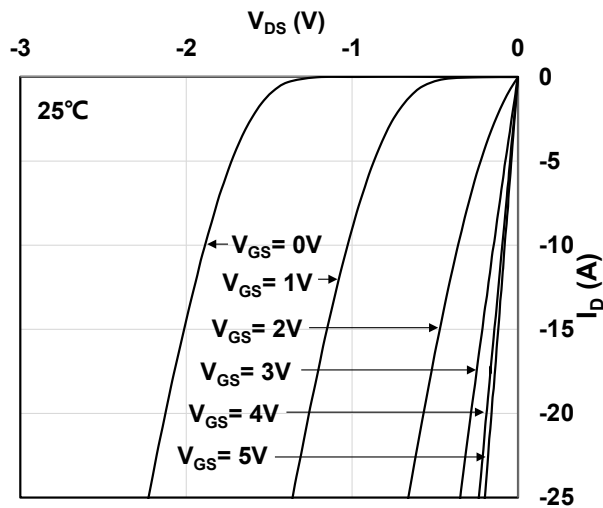
$I_D = f(V_{GS}, T_J); V_{DS} = 3\text{ V}$

Fig. 6 Normalized On-State Resistance vs. Temp.



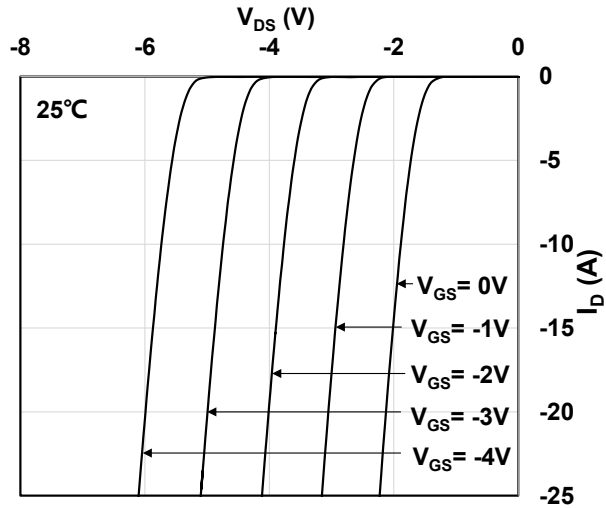
Normalized $R_{DS(on)} = f(T_J); I_D = 16\text{ A}$

Fig. 7 Typ. Reverse Drain-Source Characteristics



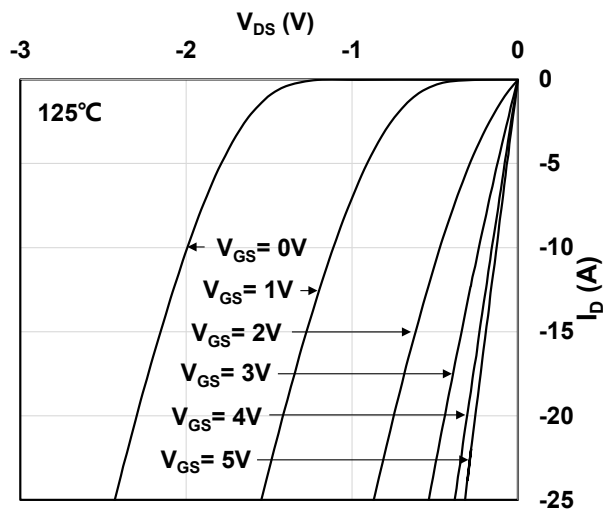
$I_D = f(V_{DS}, V_{GS}); T_J = 25\text{ }^\circ\text{C}$

Fig. 8 Typ. Reverse Drain-Source Characteristics



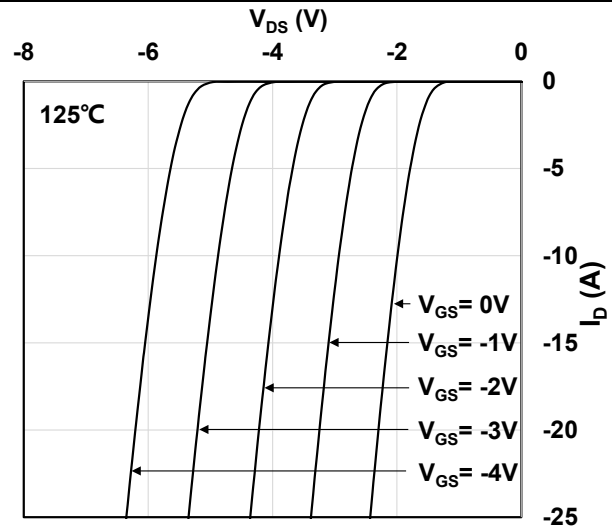
$I_D = f(V_{DS}, V_{GS}); T_J = 25\text{ }^\circ\text{C}$

Fig. 9 Typ. Reverse Drain-Source Characteristics



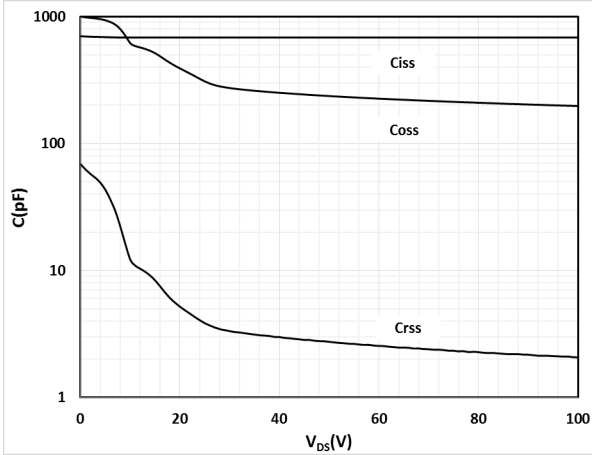
$I_D = f(V_{DS}, V_{GS}); T_J = 125\text{ }^\circ\text{C}$

Fig. 10 Typ. Reverse Drain-Source Characteristics



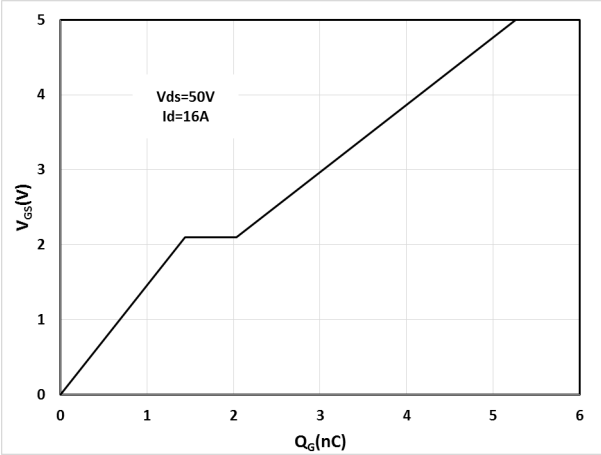
$I_D = f(V_{DS}, V_{GS}); T_J = 125\text{ }^\circ\text{C}$

Fig. 11 Typ. Capacitances(Log Scale)



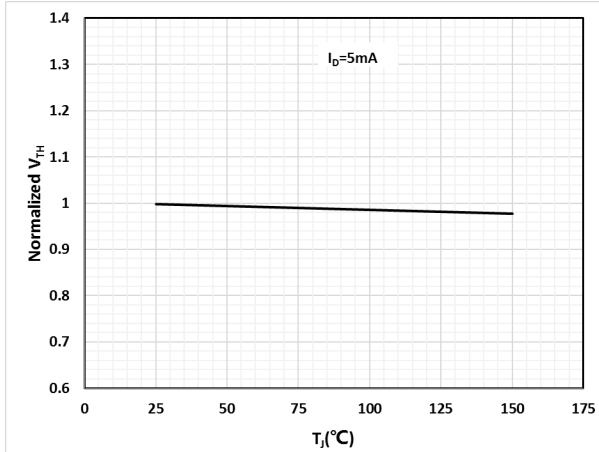
$I_D = f(V_{DS}, V_{GS}); T_J = 25\text{ }^\circ\text{C}$

Fig. 12 Typ. Gate Charge



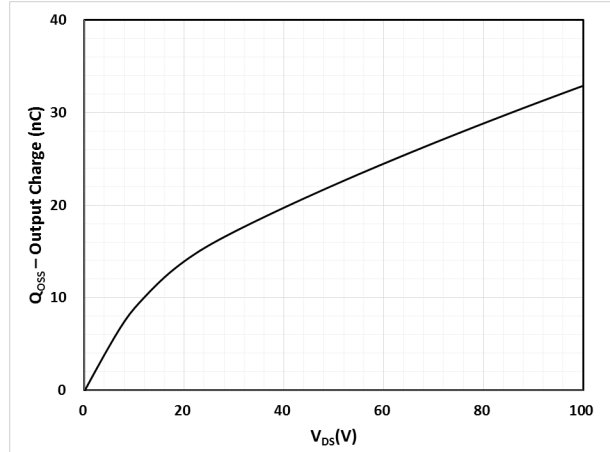
$V_{GS} = f(Q_G); V_{DS} = 50\text{ V}; I_D = 16\text{ A}$

Fig. 13 Normalized Threshold Voltage vs. Temp.



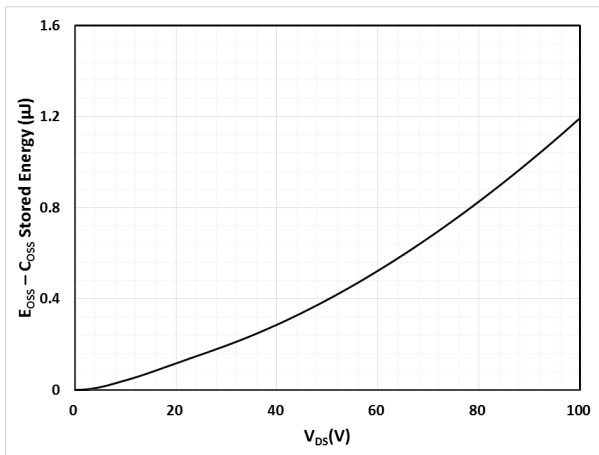
Normalized $V_{TH} = f(T_J)$; $V_{GS} = V_{DS}$; $I_D = 5\text{ mA}$

Fig. 14 Output Charge



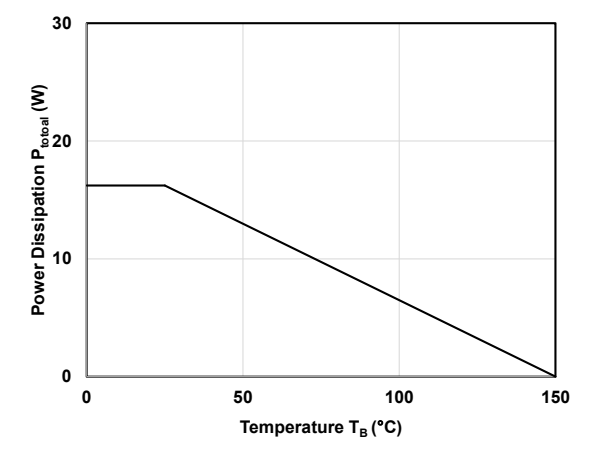
$Q_{OSS} = f(V_{DS})$

Fig. 15 Output Capacitance Stored Energy



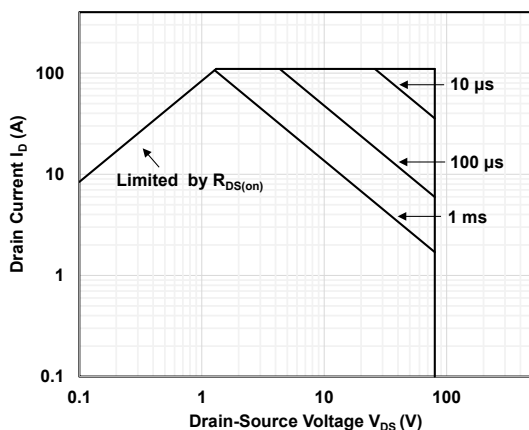
$E_{OSS} = f(V_{DS})$

Fig. 16 Power Dissipation



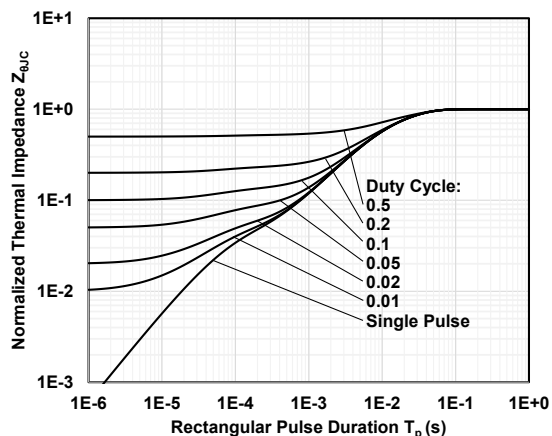
$P_{TOT} = f(T_B)$

Fig. 17 Safe Operating Area



$I_D = f(V_{DS}); T_B = 25\text{ }^\circ\text{C}; \text{Single Pulse}$

Fig. 18 Max. Transient Thermal Impedance



$Z_{\theta JB} = f(t_p); \text{parameter: } D = t_p / T$

Marking Reference

Marking Line 1 (INN)	Innoscence
Marking Line 2 (J12)	INN100L12
Marking Line 3 (YYY)	Lot Code
Marking Line 4 (YYY)	

Package Reference (units in μm)

DIM	MICROMETERS		
	MIN	NOM	MAX
a	2590	2640	2690
b		1045	
c		130	
d		1550	
e		120	
f		565	
g	200	250	300
h	1900	1950	2000
i	625	675	725
j	465	515	565
k	2800	2900	3000
l	1800	1900	2000
m	260	310	360
n		550	
o	170	200	230
p	690	750	810

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